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Synchronization for an MMC Distributed Control System Considering Disturbances Introduced by Sub-module Asynchrony

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Abstract—The modular multilevel converter (MMC) is a promising topology for HVDC applications, which typically adopts a distributed control architecture to manage considerable sub-modules (SMs) in the system. SM synchronization is necessary for an MMC distributed control system to cope with the local controller clock discrepancy and asynchrony due to the manufacturing tolerance. This paper proposes a synchronization scheme for the MMC distributed control system taking the disturbances introduced by the SM asynchrony into account. The MMC models considering SM asynchrony reveal that the asynchrony introduces harmonics around the carrier frequency in MMC output and the circulating current. The interaction between the SM switching harmonics and arm current harmonics leads to divergence of the capacitor voltages. The MMC distributed control system cannot entirely restrain the voltage divergence and maintain the system stability owing to the control capability saturation of the balancing controller. According to the theoretical analysis, the synchronization interval is properly selected considering the harmonic contents in the MMC output, the capacitor voltage deviation, and the distributed control system stability. The theoretical models and the proposed synchronization scheme are validated experimentally on an MMC prototype.

Index Terms—Modular Multilevel Converter, distributed control, synchronization scheme, sub-module asynchrony.

I. INTRODUCTION

THE modular multilevel converter (MMC) has been an emerging and highly efficient solution for high voltage power conversion in recent years [1] and it is gaining more and more attention because of its prominent advantages compared with conventional two-level or three-level voltage source converters. These advantages such as modularity, flexible expandability, transformer-less configuration, common dc bus, and high reliability due to redundancy, make the MMC the most promising topology for high-voltage high-power applications, especially in the high-voltage direct current transmission (HVDC) sector [2, 3] and medium voltage micro-grids [4-6]. In HVDC

applications, hundreds of SMs are typically required for the MMCs to handle a high voltage (hundreds of kilovolts) with relatively low-voltage rating power devices. In favor of properly manipulating such large number of SMs, distributed controls with phase-shifted (PS) PWM scheme for MMCs are proposed in [7-11], in order to improve the modularity of the MMC system in terms of software and distributing the computational burden into different digital controllers. However, an inherent problem along with a distributed control system for MMCs is the asynchrony of SM controllers, due to the manufacturing tolerance of crystal oscillators that provide controller clocks. The asynchronous local controllers increase the switching harmonics of an MMC adopting the PS-PWM scheme, distort the output voltage waveform, lead to capacitor voltage variation, and eventually deteriorate the performance of the overall MMC system.

Various synchronization methods have been designed for distributed systems in existing research works. A global synchronization method with gradually changed phase-shift angle for the distributed inverters is proposed in [12], in order to attenuate the high-frequency harmonics in the output current. The influence of the phase-leg modules asynchrony to the SVPWM scheme for an inverter is investigated in [13], and non-characteristic harmonic components are introduced into the line-to-line output voltage because of the modules asynchrony. The method to synchronize and control a system of parallel single-phase inverters without communication is presented in [14]. The above studies are of interest to more general distributed control systems but might be applied to MMCs as well. Synchronization methods based on CAN-bus and EtherCAT in an MMC distributed control system are addressed in [15, 16], respectively. The synchronization strategies adopted for a communication burden reduced MMC distributed control system are designed in [8, 9], and the synchronization interval is chosen as 20 ms corresponding to the fundamental frequency. Attention should be paid that the time intervals between two adjacent synchronization signals in the aforementioned researches are all arbitrarily selected without theoretical analysis. An irrational synchronization interval might result in either heavy communication burden or system performance deterioration. Thus, it is crucial to design the synchronization scheme and interval according to the influence introduced by the SM asynchrony.

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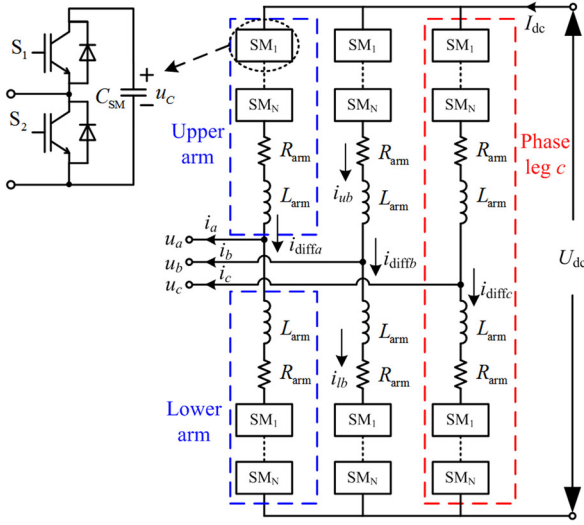


Fig. 1. Structure of a three-phase MMC.

In this paper, a synchronization scheme for the MMC distributed control system is elaborately designed, in order to alleviate the communication burden for synchronization while achieving a stable operation. The synchronization interval is selected considering the disturbances introduced by the SM asynchrony in the MMC distributed control system. For the sake of a properly designed synchronization scheme, the MMC system with SM asynchrony has to be modeled and studied. The proposed models reveal that the SM asynchrony introduces extra harmonics around the carrier frequency in the circulating current. The interaction between individual SM output switching harmonics and arm current harmonics leads to capacitor voltage diverging, which might exceed the safe operation area of SM capacitors. Moreover, such voltage diverging introduces a disturbance into the voltage balancing controller and makes the output of the controller to grow with time. Consequently, the damping capability of the balancing controller on the capacitor voltage diverging would eventually be limited by the preset control-output saturation, which results in system instability. Thus, the impact of SM asynchrony is not able to be eliminated in terms of control and a proper synchronization scheme is necessary for the MMC distributed control system. Based on the findings, a synchronization interval design method considering the harmonic requirements of the MMC output, the safety range of capacitor voltage deviation, and the system stability is proposed. The rationality of the theoretical analysis and the effectiveness of the synchronization scheme are experimentally verified on an MMC prototype in the laboratory. The experimental and simulation results confirm that the MMC system operates properly and stably in both steady-state and large step changes scenarios under the proposed synchronization method and the communication burden is largely eased compared with the traditional ones.

II. BASIC OPERATING PRINCIPLES OF MMC

A. Operation principle of an MMC

The basic structure and operation principles of an MMC have been extensively explained in the literature [17, 18] and will not be detailed in this paper. The circuit configuration of a three-

phase MMC is shown in Fig. 1. There are three phase legs connected in parallel to a common dc bus. Each phase leg consists of two arms, named as the upper and lower arm, which are connected through buffer inductors. Each arm is formed by a series connection of N identical half-bridges, termed submodules (SMs) and each SM contains a dc capacitor and two insulated gate bipolar transistors (IGBTs). As shown in Fig. 1, each arm is equipped with an arm inductor L_{arm} . An equivalent resistor R_{arm} is employed in each arm to represent the arm losses. The output terminals of the MMC are the middle points of the two arms in the three phase legs.

B. Mathematical Model of an MMC

The insertion indices indicate the relative number of SMs that should be inserted in each arm which are denoted as n_u for the upper arm and n_l for the lower arm. According to the principle of the MMC, if the output voltage is $u_o = U_o \cos(\omega_o t)$, the ideal SM insertion index is given as

$$\begin{aligned} n_u &= 0.5[1 - m \cos(\omega_o t)] \\ n_l &= 0.5[1 + m \cos(\omega_o t)] \end{aligned} \quad (1)$$

where m is the modulation index defined as $2U_o/U_{dc}$, ω_o is the angular frequency of the MMC output voltage.

The arm currents are denoted as i_l for the lower arm and i_u for the upper arm, respectively. The arm currents are defined such that a positive arm current is charging the capacitors. Ideally, the phase current splits equally into these two arms and the arm currents in Fig. 1 are given by

$$\begin{aligned} i_u &= i_{diff} + 0.5i_o \\ i_l &= i_{diff} - 0.5i_o \end{aligned} \quad (2)$$

where i_{diff} denotes the circulating current flowing between the dc terminals and i_o is the alternating phase current flowing through the ac terminal. The circulating current is directly related to the difference between the dc-link voltage and the sum of the inserted voltages in the arms [19, 20]. Equation (3) can be obtained according to the Kirchhoff's voltage law

$$L_{arm} \frac{di_{diff}}{dt} = \frac{1}{2}U_{dc} - \frac{u_l + u_u}{2} - R_{arm}i_{diff} \quad (3)$$

where U_{dc} is the dc-link voltage, u_l and u_u are the inserted voltages in the lower and upper arm, respectively.

III. MMC SYSTEM WITH SM ASYNCHRONY

A. Switching function for total voltage in a phase leg

The distributed control system for an MMC consists of a central controller and local controllers distributed in SMs [8]. Phase-shifted triangular carriers for the PS-PWM are separately implemented in local controllers. It is rational to consider that the manufacturing tolerance of the independent and randomly-selected crystal oscillators for local controllers has a normal distribution. The quartz error of local controllers in an MMC with hundreds of SMs should eventually converge to the actual normal distribution since the sample size is sufficiently large [21].

The switching functions in the upper and lower arms considering the error of carrier frequencies (x_{ui}/x_{li}) are derived as

$$s_u = \frac{N}{2} - \frac{Nm}{2} \cos(\omega_o t) + \sum_{i=1}^N \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] J_n\left(\frac{mk\pi}{2}\right) \times \cos\left[k\left((1+x_{ui})\omega_c t + \alpha + \beta + (i-1)\frac{2\pi}{N}\right) + n(\omega_o t + \pi)\right]$$

$$s_l = \frac{N}{2} + \frac{Nm}{2} \cos(\omega_o t) + \sum_{i=1}^N \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{mk\pi}{2}\right) \cos\left[k\left((1+x_{li})\omega_c t + \alpha + (i-1)\frac{2\pi}{N}\right) + n\omega_o t\right] \quad (4)$$

where J_n refers to the Bessel function, ω_c is the angular frequency of the MMC triangular carrier, k is the harmonic order of the carrier and n is the harmonic order of the reference. α is the phase displacement between the carrier waves and the modulation signal, and β indicates the angular displacement between the carrier waveforms in the upper and lower arms. α and β are selected as zero for simplicity [22, 23].

Taking the upper arm as an example, the frequency error x_{ui} appears only in the last trigonometric term in equation (4). Thus, analysis is devoted to the trigonometric term. For that the frequency error x_{ui} has a negligible value (typically 10^{-5}), $kx_{ui}\omega_c t$ is assumed close to zero. Thus, the approximation $\sin(kx_{ui}\omega_c t) \approx kx_{ui}\omega_c t$ can be obtained. Based on the probability-based frequency error model proposed in [21], x_{ui} follows the normal distribution and its mean and variance values are zero and σ^2 , respectively. The detailed simplification of (4) is elaborately demonstrated in [21] and would not be specified in this paper. The total switching function can be finally derived as

$$s_u \approx N \left\{ \frac{1}{2} - \frac{u_o^*}{2} + \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] J_n\left(\frac{mk\pi}{2}\right) \cos\phi_u \times \left[1 - \frac{(\sigma k \omega_c t)^2}{2} \right] - \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2|x|\omega_c t}{\pi^2} \sin\left[\frac{(k+n)\pi}{2}\right] J_n\left(\frac{mk\pi}{2}\right) \sin\phi_u \right\} \quad (5)$$

where $\phi_u = k\omega_c t + n(\omega_o t + \pi)$, $|x|$ stands for the average value of $|x_{ui}|$, σ denotes the per-unit frequency standard deviation, which can be derived according to the tolerance of crystal oscillators (f_{err} ppm) as $\sigma = f_{\text{err}}/2 \times 10^{-6}$ [21].

Considering the MMC output switching function as $s_o = (s_l - s_u)/2$, the switching function of the MMC output can be eventually derived as in (6), where $\phi = k\omega_c t + n\omega_o t$, x_u and x_l stand for the average values of the frequency error x_{ui} and x_{li} , respectively.

It should be noted that the circulating current in each phase is directly related to the sum of the switching functions of the upper and lower arms, which can be derived as

$$s_u + s_l = N + \sum_{i=1}^N \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{mk\pi}{2}\right) \times \Omega_i \quad (7)$$

where

$$\Omega_i = \cos\left[\phi + k(i-1)\frac{2\pi}{N} + kx_{li}\omega_c t\right] + \cos\left[\phi + k(i-1)\frac{2\pi}{N} + kx_{ui}\omega_c t + n\pi\right] \quad (8)$$

It has been discussed thoughtfully in [21] that the switching harmonics around relatively low frequencies (e.g. ω_c and $2\omega_c$) might significantly distort the voltage waveform. Therefore, only the low-frequency harmonics, i.e. the harmonics with a harmonic order $k < N$, are considered in the calculation. It should be noted that the simplification of (8) depends on the parity of n . Therefore, equation (7) can eventually be derived as

$$s_u + s_l = N + \sum_{k=1}^{k/N \in \mathbb{N}^+} \sum_{n=-\infty}^{\infty} (-1)^{n+1} \frac{2N}{\pi^2} \sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{mk\pi}{2}\right) \left| x_u + (-1)^n x_l \right| \omega_c t \sin\phi \quad (9)$$

B. Circulating current under SM asynchrony

According to the operation principle of MMC, the circulating current is directly related to the difference between the dc-link voltage and the sum of the inserted voltages in the arms [20]. Ignoring the impact from parasitic arm resistance R_{arm} and assuming an equal distribution of individual capacitor voltages U_{Cui} , i.e., U_{Cui} approximately equals U_{dc}/N , the circulating current can be derived as

$$i_{\text{diff}} = i_{\text{diff_dc}} - \frac{U_{\text{dc}}}{2L_{\text{arm}}N} \int (s_{hu} + s_{hl}) dt \quad (10)$$

where s_{hu} and s_{hl} stand for the harmonic components in the upper and lower arm switching functions, respectively. $i_{\text{diff_dc}}$ denotes the dc component in the circulating current. Ideally, the phase current i_o would split equally into the two arms [18] and the even-order circulating current ripples are well-suppressed [20, 24], the upper arm current i_u can be expressed as

$$i_u = \frac{i_o}{2} + i_{\text{diff_dc}} + \frac{\omega_c U_{\text{dc}}}{\pi^2 L_{\text{arm}}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} (-1)^n \times \left| x_u + (-1)^n x_l \right| \times \sin\left[\frac{(k+n)\pi}{2}\right] J_n\left(\frac{mk\pi}{2}\right) \times \frac{\sin\omega_h t - \omega_h t \cos\omega_h t}{\omega_h^2} \quad (11)$$

where $\omega_h = k\omega_c + n\omega_o$. The last trigonometric terms in equation (11) can be rewritten as

$$\frac{\sin\omega_h t - \omega_h t \cos\omega_h t}{\omega_h^2} = \frac{\sqrt{1+\omega_h^2 t^2}}{\omega_h^2} \sin(\omega_h t - \theta) \quad (12)$$

where $\theta = \arctan(\omega_h t)$. For that ω_h is rather large, $\theta \approx \pi/2$ and $\omega_h^2 t^2 \gg 1$ can be obtained. (11) can be further simplified as

$$i_u = \frac{i_o}{2} + i_{\text{diff_dc}} - \frac{\omega_c U_{\text{dc}}}{\pi^2 L_{\text{arm}}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} (-1)^n \frac{t}{\omega_h} \times \left| x_u + (-1)^n x_l \right| \times \sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{mk\pi}{2}\right) \times \cos\omega_h t \quad (13)$$

It can be deduced from (13) that harmonics, whose dominant

$$s_o \approx \frac{Nu_o^*}{2} + \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{N}{2\pi^2} \sin\left[\frac{(k+n)\pi}{2}\right] J_n\left(\frac{mk\pi}{2}\right) \left\{ \left[1 + (-1)^n \right] \left| x_u - x_l \right| - \left[1 + (-1)^{n+1} \right] \left| x_u + x_l \right| \right\} \omega_c t \sin\phi$$

$$+ \sum_{k=1}^{k/N \in \mathbb{N}^+} \sum_{n=-\infty}^{\infty} \frac{N}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] J_n\left(\frac{mk\pi}{2}\right) \left[1 + (-1)^{n+1} \right] \left[1 - 0.5(k\omega_c \sigma t)^2 \right] \cos\phi \quad (6)$$

components are the ones around the carrier frequency, are introduced into the arm current due to the SM asynchrony. Similar arm current for the lower arm can be derived.

C. Capacitor voltage deviation due to SM asynchrony

It should be noted that the switching frequency of the individual SM is actually the carrier frequency. Thus, the SM switching harmonics would couple with those in the circulating current around the same frequency and produce a dc offset in the capacitor current. The current flowing through the capacitor in the i^{th} SM can be expressed as the product of the switching function and the arm current.

$$\begin{cases} i_{Cui} = s_{ui} i_u \\ i_{Cli} = s_{li} i_l \end{cases} \quad (14)$$

Substituting s_{ui} and i_u into (14), as

$$s_{ui} i_u = \left\{ \frac{1}{2} - \frac{u_o^*}{2} + \left[\sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} (-1)^n \times \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] J_n\left(\frac{mk\pi}{2}\right) \right] \times \cos\left[k(i-1)\frac{2\pi}{N} + \omega_h t\right] \right\} \quad (15)$$

It should be made clear that only the dc component in (15) contribute to the capacitor voltage shifting. The switching harmonics around the carrier frequency ω_c would couple with those in the arm current having the same frequencies and consequently generate a small amount of dc current that diverges the SM capacitor voltages. Noting that the actual carrier frequency of an SM is $(1 + x_{ui})\omega_c$ and x_{ui} has an order of 10^{-5} , it is rational to neglect x_{ui} without introducing significant influence to the capacitor dc current that is mainly induced by harmonics around ω_c . Thus, the dc component in (15) is derived as

$$\begin{aligned} (s_{ui} i_u)_{dc} &= \frac{i_{diff,dc}}{2} - \frac{mI_o \cos \varphi}{4} \\ &- \frac{\omega_c U_{dc}}{\pi^3 L_{arm}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{t}{k\omega_h} \times \left[x_u + (-1)^n x_l \right] \\ &\times \sin^2\left[\frac{(k+n)\pi}{2}\right] \times J_n^2\left(\frac{mk\pi}{2}\right) \times \cos\left[k(i-1)\frac{2\pi}{N}\right] \end{aligned} \quad (16)$$

Given that the first two terms in (16) cancel each other out in the steady-state based on the power balancing in MMC [18],

the dominate dc component in (16) is introduced by the harmonic component around the carrier frequency in the switching function and the arm current. The capacitor voltage deviation caused by SM asynchrony can be derived by integrating the current flowing through the capacitor and dividing it by the capacitance C_{SM} , as

$$\begin{aligned} \Delta U_{Cui} &= -\frac{\omega_c U_{dc}}{2\pi^3 L_{arm} C_{SM}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{k\omega_h} \left[x_u + (-1)^n x_l \right] \\ &\times \sin^2\left[\frac{(k+n)\pi}{2}\right] J_n^2\left(\frac{mk\pi}{2}\right) \cos\left[k(i-1)\frac{2\pi}{N}\right] \times t^2 \end{aligned} \quad (17)$$

Whereas the dc component in individual capacitor voltage can eventually be derived as

$$U_{Cui} = \frac{U_{dc}}{N} + \Delta U_{Cui} \quad (18)$$

It can be seen from (17) that the capacitor voltage deviations are mainly determined by the dc-side voltage, the carrier frequency, the crystal oscillator tolerance, and the circuit parameters such as the arm inductance and the SM capacitance. The value and direction of ΔU_{Cui} are determined by the value of $\sin[k(i-1)2\pi/N + \pi/2]$ depending on the sequence of SMs. It implies that the capacitor voltages will differ from each other due to the different values and directions of voltage deviations. Also the voltage diverging is directly related to the square of the frequency error accumulating period, which means that the capacitor voltage might diverge dramatically and significantly deteriorate the control performance of the capacitor voltage balancing loop, and eventually lead to the malfunction of the MMC in a short period of time. It is worth noting that the capacitor voltage deviations are not considered while calculating the circulating current ripple in (10). The approximate model is adopted to sufficiently evaluate the SM capacitor voltage deviation with simplicity in this paper. A model deliberating the capacitor voltage variation and the corresponding reference change could give a more accurate calculation of the voltage deviation.

IV. MMC DISTRIBUTED CONTROL SYSTEM WITH SM ASYNCHRONY

The control tasks of the distributed control strategy for the MMC are assigned to different controllers, i.e., a central controller and local controllers located in SMs [8]. The output power and current controls are implemented in the central controller. Whereas the average capacitor voltage control, differential current regulation, and capacitor voltage balancing are completely distributed into local controllers.

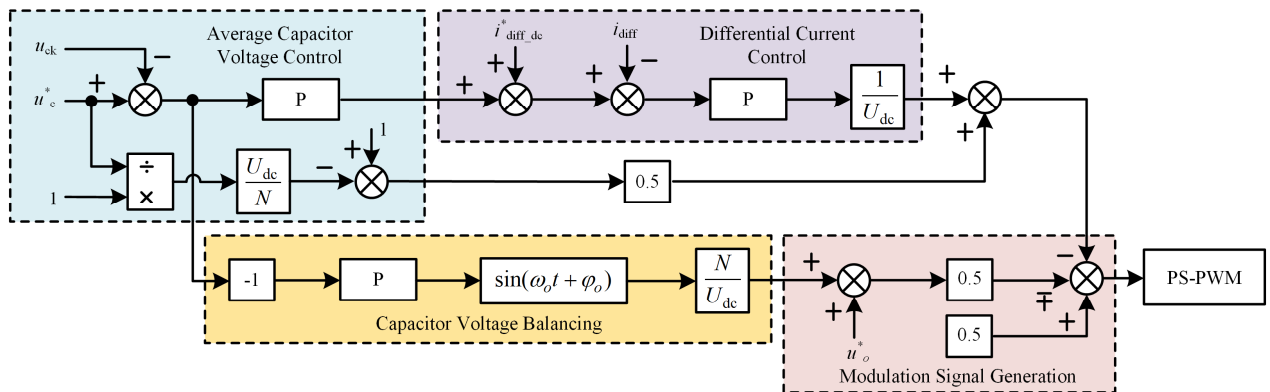


Fig. 2. Block diagram of the distributed control MMC.

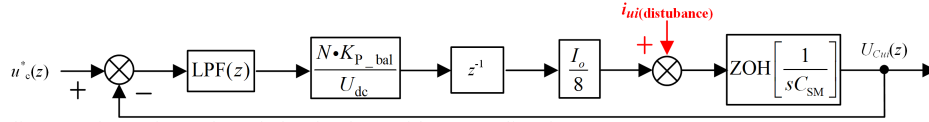


Fig. 3. Simplified block diagram of capacitor voltage-balancing loop with current disturbance.

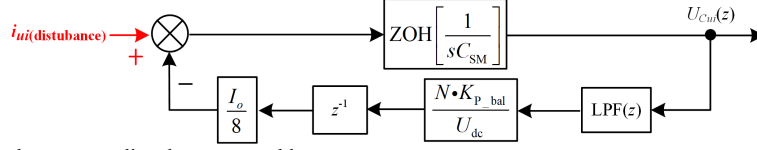


Fig. 4. Block diagram of the equivalent current disturbance control loop.

The block diagram of the control loops in the local controllers is shown in Fig. 2. The basic structure and operation principles of an MMC with distributed control have been extensively explained in the literature [8, 9] and will not be discussed in this paper. It should be noted that since the output current regulation is not the main concern in this paper, the output current control implemented in the central controller is not shown in Fig. 2. In this section, the performance and stability of the distributed control system with SM asynchrony is theoretically analyzed.

A. Circulating current control

The current circulating in each phase legs mainly includes a dc component, whose reference is set to be $U_o I_o \cos(\phi_o)/(2U_{dc})$ for the power balancing, and a dominant second-order harmonic component [25, 26]. The normally implemented circulating current control strategies target at eliminating or restraining the second-order harmonics [20, 27].

The circulating current controllers are mainly designed to cope with the signal at the second-order frequency and follow the dc-side current reference [8]. Thus, they are not able to suppress the relevant high-frequency harmonics around and beyond the switching frequency ω_c for individual SM.

B. Capacitor Voltage Averaging Control

The control of SM capacitor voltage of the MMC is an unavoidable task. Thus various voltage control strategies are designed for SM voltage averaging and balancing [17, 28].

Capacitor average voltage control loop aims at controlling the average capacitor voltage in each phase according to the reference u_c^* given by the central controller. The average voltage is obtained by summing up the capacitor voltages in each phase then divided with $2N$, which is expressed as

$$\bar{U}_{Cu} = \frac{1}{2N} \sum_{i=1}^N (U_{Cui} + U_{Cli}) \quad (19)$$

where U_{Cli} stands for individual capacitor voltage in the lower arm. It can be observed from (19) that the averaging control actually targets at the sum of the voltage in one phase. Based on equation (17), the sum of the voltage deviations caused by SM asynchrony in the upper arm can be derived as

$$\sum_{i=1}^N \Delta U_{Cui} = \frac{\omega_c U_{dc}}{2\pi^3 L_{arm} C_{SM}} \sum_{i=1}^N \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{k\omega_h} \left[x_u + (-1)^n x_l \right] \times \sin^2 \left[\frac{(k+n)\pi}{2} \right] J_n^2 \left(\frac{mk\pi}{2} \right) \cos \left[k(i-1) \frac{2\pi}{N} \right] t^2 \quad (20)$$

The sum of the voltage deviations for the lower arm can be derived similarly. It should be noted that the sum of the last

trigonometric term of equation (20) for N SMs is actually zero, which means that the arm voltage deviation would eventually yield to zero. Therefore, the SM asynchrony would not affect the capacitor voltage average control.

C. Capacitor Voltage Balancing Control

The voltage balancing control strategies are utilized to adjust and balance the individual SM capacitor voltages. Various schemes have been proposed for MMC system stability analysis [29, 30], the frequency domain analysis utilizing control loop transfer function is adopted in the paper. A simplified block diagram of the capacitor voltage-balancing loop for the i th SM can be found in Fig. 3, where the LPF block stands for the low pass filter, K_{p_bal} denotes the proportional gain of the voltage balancing control, while I_o is the amplitude of the alternating output current.

Noting that the dc components in the capacitor current contribute to the shifting of the capacitor voltage, the dc capacitor current caused by SM asynchrony can be deemed as a disturbance to the voltage-balance control loop showing in Fig. 3. As discussed in section II, such current disturbance can be quantitatively derived in the frequency-domain as

$$i_{iii}(\text{disturbance}) = s \Delta U_{Cui}(s) C_{SM} = \frac{\omega_c U_{dc}}{\pi^3 L_{arm}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{k\omega_h} \left[x_u + (-1)^n x_l \right] \times \sin^2 \left[\frac{(k+n)\pi}{2} \right] \times J_n^2 \left(\frac{mk\pi}{2} \right) \times \cos \left[k(i-1) \frac{2\pi}{N} \right] \times \frac{1}{s^2} \quad (21)$$

The block diagram of the closed-loop transfer function from the current disturbance $i_{iii}(\text{disturbance})$ to the capacitor voltage U_{Cui} is depicted in Fig. 4. The closed-loop transfer function can be derived accordingly

$$\phi(s) = \frac{1}{s C_{SM} + \frac{N I_o K_{p_bal}}{8 U_{dc}}} \quad (22)$$

It can be seen that the disturbance from the capacitor current is a second-order element as in (21), and the closed-loop transfer function for the current disturbance in (22) has no s in its numerator. Based on the control theory, the steady-state error of the disturbance suppression loop is given as

$$e_{ss} = \lim_{s \rightarrow 0} s \cdot \phi(s) \cdot i_{iii}(\text{disturbance})(s) = \infty \quad (23)$$

Equation (23) reveals that the steady-state capacitor voltage error caused by the harmonic current disturbance would finally diverge to infinite and lead to a system breakdown. It should be noted that a proportional-integral (PI) controller, which has a

one-order s in its close-loop transfer function numerator, is theoretically able to restrain the disturbance caused by the capacitor current according to equation (23). However, the capacitor voltage could be easily unstable by utilizing a PI controller in the capacitor voltage control loops, due to the control conflict among different SMs in one phase leg [8].

In order to evaluate the performance of the voltage balance control, the capacitor voltage deviation taking the capacitor voltage control into account is derived as

$$\delta U_{Cui}(s) = \frac{A_i}{s^2} \frac{8U_{dc}}{8U_{dc} s C_{SM} + NI_o K_{P_bal}} \quad (24)$$

where A_i is given as

$$A_i = \frac{\omega_c U_{dc}}{\pi^3 L_{arm}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{k \omega_h} \overline{x_u + x_l} \times \sin^2 \left[\frac{(k+n)\pi}{2} \right] \times J_n^2 \left(\frac{mk\pi}{2} \right) \times \cos \left[k(i-1) \frac{2\pi}{N} \right] \quad (25)$$

The capacitor voltage deviation in the time-domain is derived by taking the inverse Laplace transform of equation (24).

$$L^{-1}[\delta U_{Cui}(s)] = \left(\frac{8A_i U_{dc}}{NI_o K_{P_bal}} \right) \times \left[\left(\frac{8C_{SM} U_{dc}}{NI_o K_{P_bal}} \right) e^{-\frac{NI_o K_{P_bal}}{8C_{SM} U_{dc}} t} + t - \left(\frac{8C_{SM} U_{dc}}{NI_o K_{P_bal}} \right) \right] \quad (26)$$

It should be noted that the term contains natural exponential function in (26) would drop to a negligible value after a short transient period. Hence, the dominant capacitor voltage deviation is eventually given as

$$\delta U_{Cui} \approx \left(\frac{8A_i U_{dc}}{NI_o K_{P_bal}} \right) \left(t - \frac{8C_{SM} U_{dc}}{NI_o K_{P_bal}} \right) \quad (27)$$

As indicated by equation (27), the capacitor voltage deviations mainly related to the dc-side voltage, the amplitude of the alternating output current, the number of SMs, the standard deviation of the quartz tolerance, the carrier frequency, the accumulating time of frequency error, and the voltage-balance control parameter. It can be observed that the voltage balancing controller has a damping effect on the capacitor voltage diverging, as the control parameter K_{P_bal} is in the denominator. And the order of t is also reduced compared with that in (17).

V. PROPOSED SYNCHRONIZATION SCHEME

The synchronization scheme among different local controllers in the adopted MMC distributed control system is realized based on the communication network, which is similar to the methods used in [8, 9]. A synchronization message, which contains the instant time register value of the central controller is broadcasted by the central controller through Ethernet every T_s second, where T_s is the synchronization interval. After receiving the message, local controllers would simultaneously record the local time register value and reset their carrier phase angles according to the calculated register value deviations. The design of the synchronization interval is detailed in this section considering constraints on harmonic contents, capacitor voltage deviation, and the balancing controller capability.

A. Synchronization interval selection by switching harmonics

The derived switching harmonics in the output voltage would eventually inject harmonic current into the grid and thus deteriorate the performance of the system. The harmonic components in the output switching function can approximately evaluate the switching harmonics in the MMC output voltage. The IEEE-519 standard is proposed by IEEE societies as the recommended requirements for harmonic control in electrical power systems. According to the requirement in the standard, a total harmonic distortion (THD) below 5% of the fundamental voltage value is typically required for general systems.

Based on the analysis in Section III, significant harmonics in the output switching function are generated around the carrier frequency due to the SM asynchrony. Note that the RMS value of the harmonic components can be obtained according to equation (6). Since the THD of the MMC output switching function is positively related to the error accumulating time, the maximum synchronization interval can be obtained based on the THD requirements for an MMC distributed control system.

B. Synchronization interval selection by capacitor voltage deviation

According to the analysis in Section III and Section IV, without SM synchronization, the adopted distributed control system is actually not able to restrain the capacitor voltage diverging generated by the SM asynchrony and the capacitor voltage deviations would accumulate with time and eventually cause the malfunction of the MMC system.

With the findings, suitable synchronization interval could be identified according to the worst case that the capacitor voltage balancing control is disabled. Equation (17) in Section III can be utilized to derive the maximum synchronization interval by considering

$$\left| \frac{\Delta U_{Cui}}{U_{dc} / N} \right| \leq \eta (\Delta U_{max}) \quad (28)$$

where $\eta(\Delta U_{max})$, which denotes the allowed maximum capacitor voltage deviation ratio, should be obtained according to the operation requirements in the adopted MMC system.

C. Synchronization interval selection by control saturation

Based on the study in Section III and Section IV, the outputs of the voltage balancing controllers continuously increase since the voltages keep diverging due to the SM asynchrony. The outputs of the balancing controllers grow with the error accumulating time and would be limited to the preset control-output saturation value, which eventually leads to control performance deterioration. Based on the voltage deviations in equation (17) and the balance control diagram in Fig. 3, the output of the voltage balance controller is derived as

$$\Delta s_{balance} = \frac{\omega_c K_{P_bal} N}{2\pi^3 L_{arm} C_{SM}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{k \omega_h} \overline{x_u + (-1)^n x_l} \times \sin^2 \left[\frac{(k+n)\pi}{2} \right] J_n^2 \left(\frac{mk\pi}{2} \right) \cos \left[k(i-1) \frac{2\pi}{N} \right] \times t^2 \quad (29)$$

Assuming that the control limit for the capacitor voltage balancing is s_{b_max} , the maximum synchronization interval based



Fig. 5. A down-scaled laboratory prototype of MMC.

TABLE I
EXPERIMENTAL PARAMETERS

Parameters	Experimental setup
Number of SMs: N	6 per arm
DC-link voltage: U_{dc}	300 V
Modulation index: m	0.8
Arm inductance: L_{arm}	5 mH
SM capacitance: C_{SM}	940 μ F
Carrier frequency: f_c	1 kHz
Load resistance: R_l	30 Ω

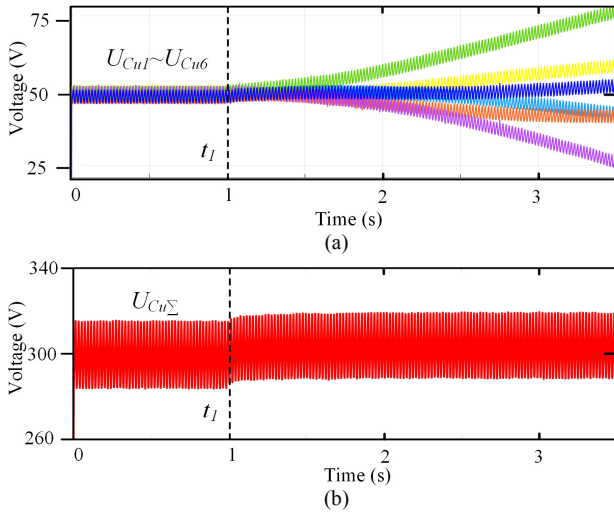


Fig. 6. Experimental waveforms of the open-loop MMC system for one phase with asynchrony: (a) individual capacitor voltages; (b) arm voltage.

TABLE II
EXPERIMENTAL AND CALCULATION RESULTS

	Experiment	Calculation
$ \Delta U_{Cmax} _{0.5s}$	3.13 V	3.13 V
$ \Delta U_{Cmax} _{1s}$	8.43 V	12.5 V
$ \Delta U_{Cmax} _{1.5s}$	15.97 V	28.2 V

on the capacitor voltage balancing control saturation can be obtained by calculating

$$|\Delta s_{balance}| \leq s_{b_max} \quad (30)$$

VI. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the validity of the mathematical analysis in the previous sections, a single-phase MMC prototype with six SMs per arm is configured based on the MMC platform shown in Fig. 5, whose detailed parameters are specified in TABLE II. The equivalent switching frequency of the MMC is $6f_c = 6$ kHz. Six DSP TMS320F28335 development boards are used as local controllers and generate PWM signals with asynchronous triangular carriers while a DSP TMS320F28346 development board is adopted as the central controller.

A. MMC without Capacitor Voltage Balancing Control

Fig. 6 shows the experimental results of the distributed control system without capacitor voltage balancing control, which is the worst case that the capacitor voltages diverge due to the harmonic current introduced by the SM asynchrony. It should be noted that the synchronized triangular carriers are adopted during 0 – 1 second to ensure the balance of capacitor voltages. The asynchronous triangular carrier is simultaneously introduced when $t_l = 1$ s. Fig. 6(a) presents the six capacitor voltages in the upper arm. It is observed that the individual capacitor voltages indeed diverge with the increase of the error accumulating time. The maximum voltage deviations when $\Delta t = 0.5$ s, 1 s, and 1.5 s are measured from Fig. 6(a), which are denoted as $|\Delta U_{Cmax}|_{0.5s}$, $|\Delta U_{Cmax}|_{1s}$, and $|\Delta U_{Cmax}|_{1.5s}$. In order to validate the capacitor voltage deviation calculation proposed in this paper, the experiment and calculation results are presented in TABLE II. It can be observed that the calculation results show acceptable coincidence with the experiment while $t < 1$ s. The calculations appear higher than experiments since the possibly maximum switching harmonics are taken into account to calculate the maximum voltage deviations and the damping effect of the parasitic resistance and the effects of other control loops in the MMC are ignored.

Fig. 6(b) presents the sum of the arm capacitor voltages. It can be apparently observed that even the capacitor voltages differ from each other, the sum of the arm capacitor voltages is maintained around 300 V, which is closed to the dc-bus voltage.

B. MMC with Capacitor Voltage Balancing Control

Fig. 7 presents the experimental results in the distributed control system, where the circulating current control, capacitor voltage balancing control, and capacitor voltage average control are all implemented. Fig. 7(a) shows the waveforms of individual capacitor voltages in the upper arm. It should be noted that the synchronized triangular carriers are adopted during 0 – 1 second. Comparing Fig. 7(a) with Fig. 6(a), it can be observed that the voltage deviations from t_l - t_2 are reasonably refined when the voltage balance controller is employed. Moreover, it should be noted that there is a good agreement between the theoretical analysis and the experimental results as shown in TABLE III. It can be concluded that the voltage deviations caused by the SM asynchrony can be largely reformed by the capacitor voltage balance controller.

According to the analysis in Section V, the voltage balance strategy using a proportional controller is not able to restrain the capacitor voltage deviation. Hence, the outputs of the balancing control loops would increase to preset control limits and eventually are not able to maintain the capacitor voltage around their references. The control limits of the voltage balance controllers are set to be ± 0.2 in local controllers. Based on equation (29) and (30), the control saturation of the studied MMC occurs at 0.8 s. It can be observed from Fig. 7(a) that since the SM asynchrony is introduced at t_l , the capacitor voltages keep diverging

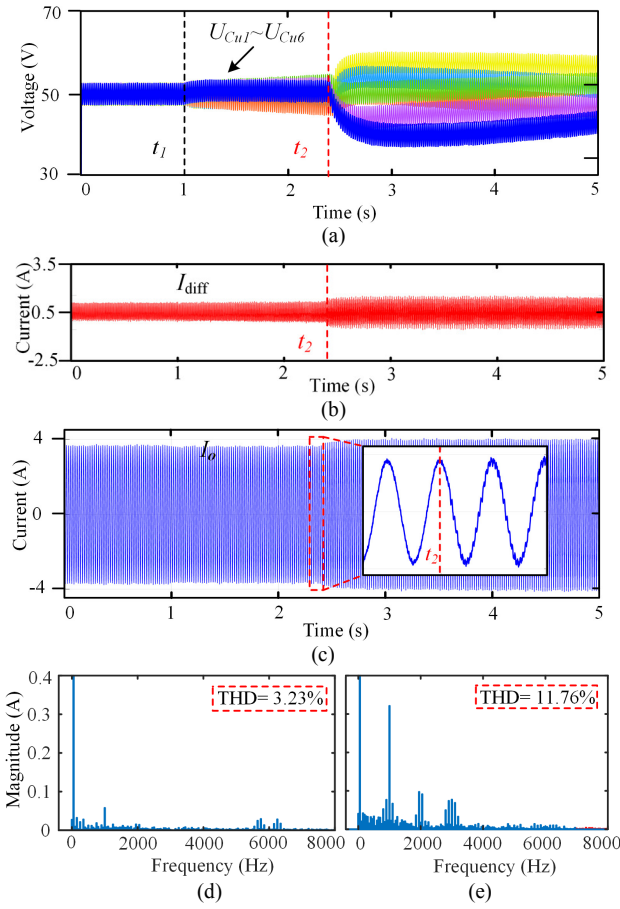


Fig. 7. Experimental waveforms of the close-loop MMC system for one phase with asynchrony: (a) individual capacitor voltages; (b) circulating current; (c) output current; (d) harmonic spectrum of output current at $t=0.5$ s; (e) harmonic spectrum of output current at $t=3$ s.

TABLE III
EXPERIMENTAL AND CALCULATION RESULTS

	Experiment	Calculation
$ \Delta U_{Cmax} _{0.5s}$	0.34 V	0.43 V
$ \Delta U_{Cmax} _{3s}$	0.68 V	0.9 V

with the error accumulating time, which also increases the outputs of voltage balance controllers. It is clearly depicted in Fig. 7(a) that the control performance was significantly deteriorated when the balance controller saturated to the preset limit at t_2 . The impact of the control saturation can also be observed from Fig. 7(b)-(c) that the circulating current and output current of the MMC system is rapidly distorted since t_2 . The harmonic spectrums of the output current in steady state ($t=0.5$ s) and the control saturation state ($t=3$ s) are presented in Fig. 7(d) and (e), respectively. It can be seen that the harmonics in output current are significantly increased after t_2 . The interval Δt between t_1 and t_2 obtained in Fig. 7(a) was 1.4 s, which quite coincides with the calculated value of 0.8 s. The slight mismatch between the two intervals could be introduced by calculating the time interval using the maximum capacitor voltages deviation.

C. MMC with Optimal Synchronization interval

Based on the criteria proposed in Section V, three synchronization intervals can be obtained. The constraint conditions and the calculated synchronization intervals are presented respectively in TABLE IV. Considering the uncertainties of the distributed control system and the inaccuracy of the mathematical

TABLE IV
CALCULATED INTERVALS IN DIFFERENT CRITERIA

	Constraint	Interval
Switching	THD $\leq 5\%$	2.5 s
Voltage deviation	$ \Delta U_{Cui}/U_{dc} \times N \leq 0.2$	0.9 s
Control saturation	$ \Delta s_{b_max} \leq 0.2$	0.8 s

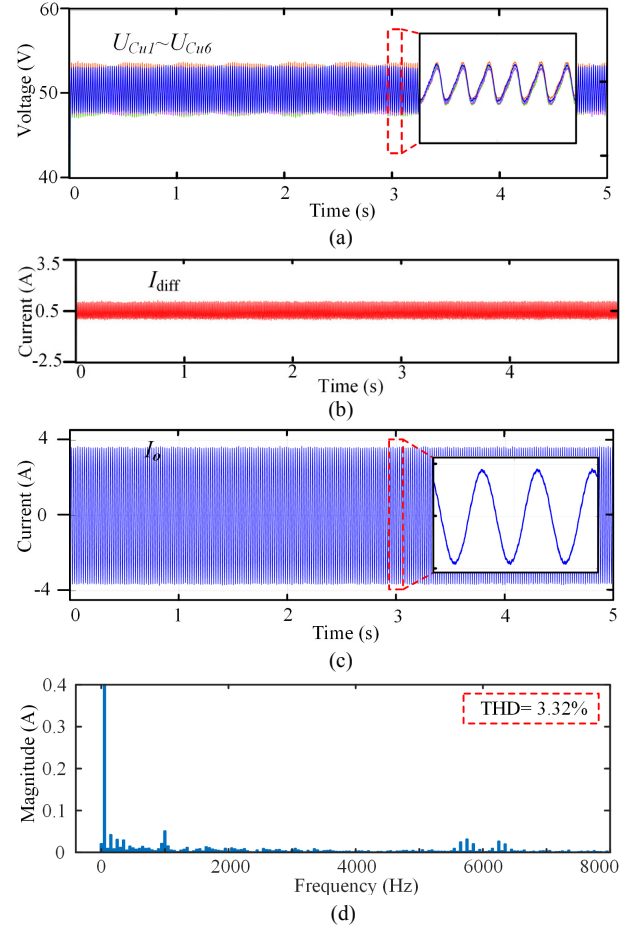


Fig. 8. Experimental waveforms of the close-loop MMC system for one phase with synchronization: (a) individual capacitor voltages; (b) circulating current; (c) output current; (d) harmonic spectrum of the output current.

models, the relevant margin is reserved and the synchronization interval for the adopted distributed control system is resolved to be 0.5 s, which means the synchronization message should be sent by the central controller every 0.5 s to re-synchronize PWM carriers of the local controllers. It should be noted that a carrier phase jump at synchronization instant after a frequency error accumulating period might distort the MMC output waveform. However, when the synchronization interval is small, the minor carrier drift tends not to introduce severe phase jump in synchronization process. In order to verify the validity of the proposed synchronization interval, the distributed MMC system synchronized with the frequency of 2 Hz is illustrated experimentally based on the same parameters in TABLE I.

The effectiveness of the synchronization is presented in Fig. 8. It can be observed that the capacitor voltage diverging in Fig. 8(a) is largely reformed because of the synchronization with the proposed interval. No severe deterioration introduced by the asynchronous switching harmonics is found in the voltage and current waveforms. Also, no evident disturbance due to the carrier phase jump is detected in the capacitor voltage and output current waveform at the synchronization instant. The maximum

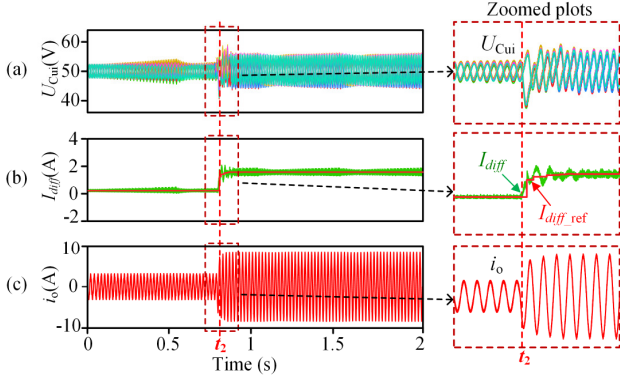


Fig. 9. Simulated waveforms of the MMC when output current reference changes from 3 to 8 A: (a) capacitor voltages; (b) circulating current and its reference; (c) output current.

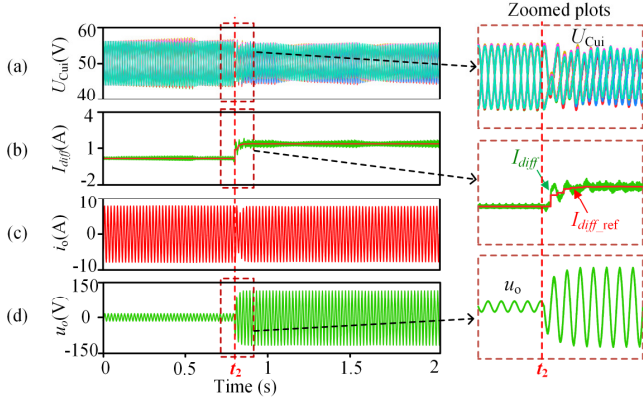


Fig. 10. Simulated waveforms of the MMC when load resistance changes from 2 to 15 Ω : (a) capacitor voltages; (b) circulating current and its reference; (c) output current; (d) output voltage.

THD value in output current is measured to be 3.32% as in Fig. 8(d), which fulfills the THD criterion in the IEEE-519 standard. Attention should be paid here that the communication burden for the synchronization signals with the proposed interval has decreased by 25 times compared with the 20 ms synchronization interval proposed in [8, 9], whereas the largely alleviated synchronization frequency makes no significant impact to the performance of the distributed MMC system according to the experimental result in Fig. 8.

D. Dynamic Response under Proposed Synchrony scheme

The dynamic responses of the periodical synchronized MMC during current reference and load resistance step changes are studied in the Piecewise Linear Electrical Circuit Simulation (PLECS) software. The MMC system configurations are identical with that in TABLE I. The synchronization interval for the 6-SM MMC is selected to be 0.5 s. The output current control

is adopted in the MMC distributed control system. The simulation waveforms of these two scenarios are presented in Fig. 9 and Fig. 10, respectively.

In Fig. 9, the output current amplitude is initially set to be 3 A and then steps to 8 A at t_1 . It can be seen from Fig. 9(c) that the output current rapidly tracks its reference and the dc component in the differential current in Fig. 9(b) is accordingly increased for the power balancing between the input and output of the MMC. The capacitor voltage deviations are always sustained in the safe ranges according to Fig. 9(a).

In the load change scenario in Fig. 10, the load resistance of the MMC is changed from 2 Ω to 15 Ω at t_2 . According to Fig. 10(c)-(d), the MMC output current is well restrained by the current controller and the output voltage is raised because of the increased load resistance. The dc component in the differential current in Fig. 10(b) is rapidly increased for power balancing. Also, no significant distortion is found in Fig. 10(a) at t_2 . The capacitor voltage deviations are maintained in the safe range.

E. Synchronization interval under system parameter varying

In order to illustrate the impact of the system parameter varying on the synchronization interval selection, graphs describing the synchronization interval t_{syn} under the three criteria in TABLE IV regarding different system parameters are depicted in Fig. 11. Notations $t_{syn}(THD)$, $t_{syn}(\Delta U_c)$, and $t_{syn}(\Delta s_b)$ indicate the synchronization intervals calculated for the output voltage THD, the capacitor voltage deviation ratio, and the balance control capability constraints. According to Fig. 11 (a), the increase of the carrier frequency leads to a decrease of $t_{syn}(\Delta U_c)$ and $t_{syn}(\Delta s_b)$, since higher carrier frequency introduces lower dc disturbance in the capacitor current. However, harmonic amplitudes become higher when carrier frequency grows, which increases the output THD and results in a lower $t_{syn}(THD)$. Based on Fig. 11 (b) and (c), when the SM numbers and frequency error are increased, t_{syn} should be smaller for that the output THD, ΔU_c , and Δs_b are more likely to exceed the preset critical values. Whereas the change of SM numbers shows no impact on the output voltage THD, since all the components of s_o in (6) are scaled by N .

Moreover, the switching harmonics and capacitor voltage deviations are both calculated considering the worst case of the SM asynchrony. And a margin would be given while selecting the system synchronization interval. Thus, it is unnecessary to frequently re-design the synchronization interval with minor parameter adjustments in the MMC system.

VII. CONCLUSION

This paper presents a sensibly-designed synchronization scheme for the MMC distributed control system, which greatly

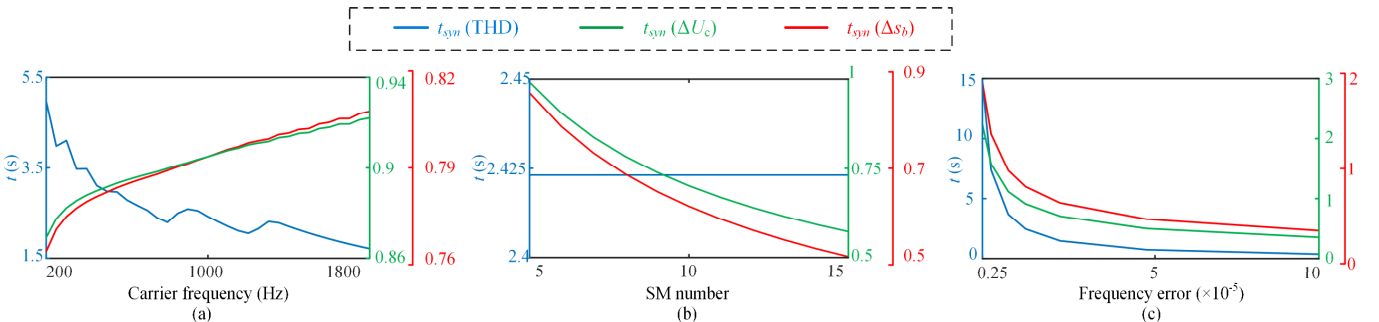


Fig. 11. Trends of synchronization intervals for output voltage THD, capacitor voltage deviation, and balance control capability constraints with varying: (a) carrier frequency; (b) SM number; (c) carrier frequency error.

relieves the communication burden for synchronization while maintaining the stable operation of the system. The MMC system with SM asynchrony is mathematically modeled and the model reveals that the SM asynchrony introduces harmonics around the carrier frequency in switching functions and the circulating current. The interaction between the switching harmonics and harmonics in arm currents around the carrier frequency leads to the capacitor voltage diverging. The capacitor voltage diverging also deteriorates the system stability due to the controller damping capability saturation. The synchronization interval is properly selected by considering the harmonic requirements, the safe operation range of the SM capacitors, and the system stability. The validity of the theoretical analysis and the effectiveness of the synchronization scheme are experimentally verified. The experimental results confirm that the mathematical model effectively represents the performance of the MMC system with SM asynchrony. Also, the MMC system operates properly and stably in steady-state and during step changes under the designed synchronization scheme with reduced data transmission.

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